Datasheet

Type 2TY Bluetooth® Low Energy Module Data Sheet

Renesas DA14531 Chipset for Bluetooth 5.1 - Rev. E

- Design Name: Type 2TY
- P/N: LBCA1HN2TY-954

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About This Document

Murata Type 2TY is a Bluetooth Low Energy module. This datasheet describes the specification of the module in detail.

Please be aware that an important notice concerning availability, standard warranty and use in critical applications of Murata products and disclaimers thereto appears at the end of this specification sheet.

Audience & Purpose

This document is intended audience includes any customer looking to integrate this module into their product. In particular, RF, hardware, software, and systems engineers.

Document Conventions

Table 1 describes the document conventions.

Table 1: Document Conventions

Conventions	Description
	Warning Note Indicates very important note. Users are strongly recommended to review.
	Info Note Intended for informational purposes. Users should review.
	Menu Reference Indicates menu navigation instructions. **Example**: Insert➔Tables➔Quick Tables➔Save Selection to Gallery
	External Hyperlink This symbol indicates a hyperlink to an external document or website. **Example**: Murata Click on the text to open the external link.
	Internal Hyperlink This symbol indicates a hyperlink within the document. **Example**: Scope Click on the text to open the link.
`Console input/output or code snippet`	**Console I/O or Code Snippet** This text ***Style*** denotes console input/output or a code snippet.
`# Console I/O comment` *`// Code snippet comment`*	**Console I/O or Code Snippet Comment** This text ***Style*** denotes a console input/output or code snippet comment. • Console I/O comment (preceded by “#”) is for informational purposes only and does not denote actual console input/output. • Code Snippet comment (preceded by “//”) may exist in the original code.

1 Scope

This specification is applied to the Bluetooth low energy module.

- Interface: GPIO (supporting UART / SPI / I2C / ADC)
- IC P/N: DA14531-FCGQFN24 (Renesas)
- Reference Clock: Internal Crystal
- Weight: 0.09 g
- MSL: Level 3
- RoHS: This component can meet with RoHS compliance.

2 Part Number

Table 2 describes the ordering part numbers.

Table 2: Ordering Information

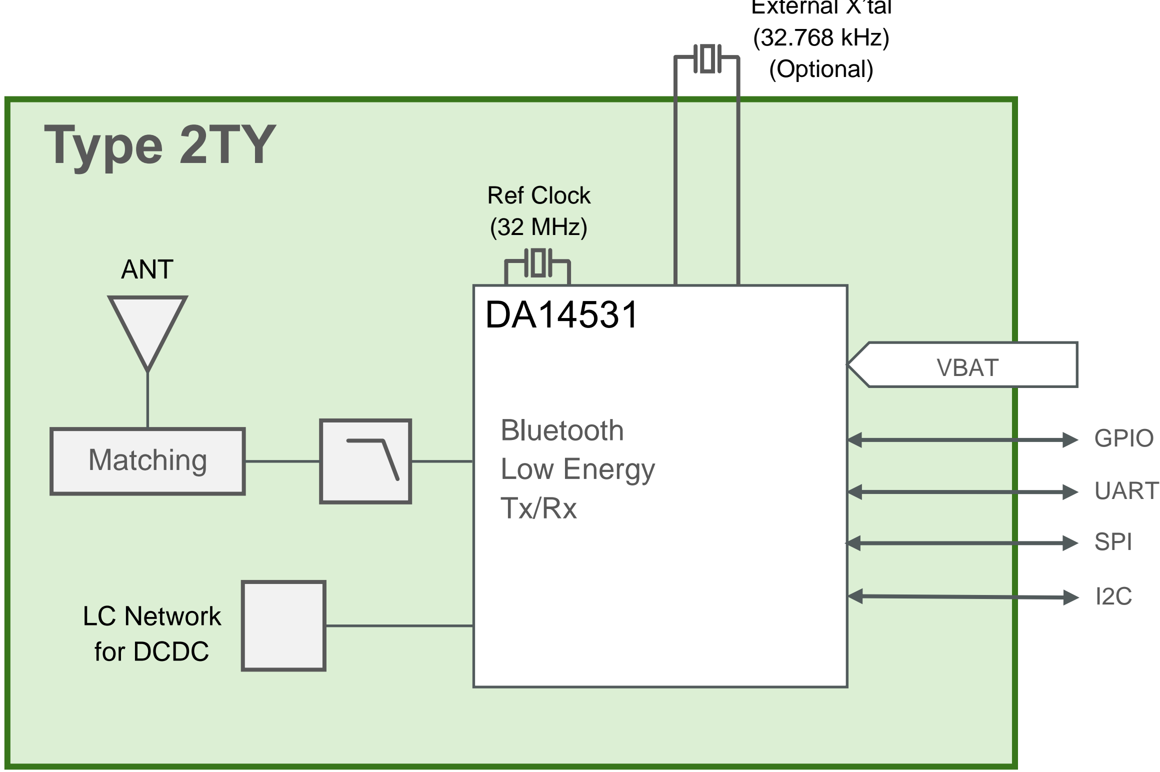
Ordering Part Number	Description
LBCA1HN2TY-954	Module order
LBCA1HN2TY-SMP	In case of sample order
LBCA1HN2TY-EVB1	Evaluation Board (EVB)

"Type 2TY" is the design name of this module. Design name may be used in certification test report.

3 Block Diagram

Figure 1 shows the block diagram.

Figure 1: Block Diagram



4 Reference

1. Dialog semiconductor, DA14531 Datasheet, v3.6, 2022

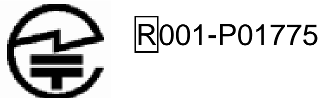
5 Certification Information

This section has certification information.

5.1 Radio Certification

This product is certified for the following regulations.

- TELEC (日本電波法)
  - Type certification （工事設計認証）



- FCC (United States) FCC Part 15 subpart C
  - Limited Modular Approval
    FCC ID: VPYLBCA2HN2AY
- IC (Canada) RSS-247

- Limited Modular Approval
  IC: 772C-LBCA2HN2AY
- CE (Europe)EN 300 328 V2.2.2
  - Conducted Test Report available

CE marking and declaration should be done by customer as a final product.

5.2 Radio Regulatory Certification by Country

Murata have prepared the document about Radio Regulatory Certification separately.

This document is designed to ensure that module manufacturers correctly communicate the necessary information to host manufacturers that incorporate their modules.

Refer to Type 2TY Radio Law Approval Application Note.

If you don't follow the rule written in Type 2TY Radio Law Approval Application Note, there is a risk of conflict Radio Law Certification.

Please be sure to check the documents.

5.3 Bluetooth® Qualification

- Bluetooth® SIG Qualifications
  Please refer to the following QDID.
  - **QDID:** 113959 (Controller Subsystem by Dialog Semiconductor (Renesas))
    - Design Name: DA14531 - Controller

Profile subsystem QDID is needed only if SIG standard profile is used.

6 Dimensions, Marking, and Terminal Configurations

Figure 2 shows the dimensions, markings, and terminal configurations.

Figure 2: Dimensions (Unit: mm)

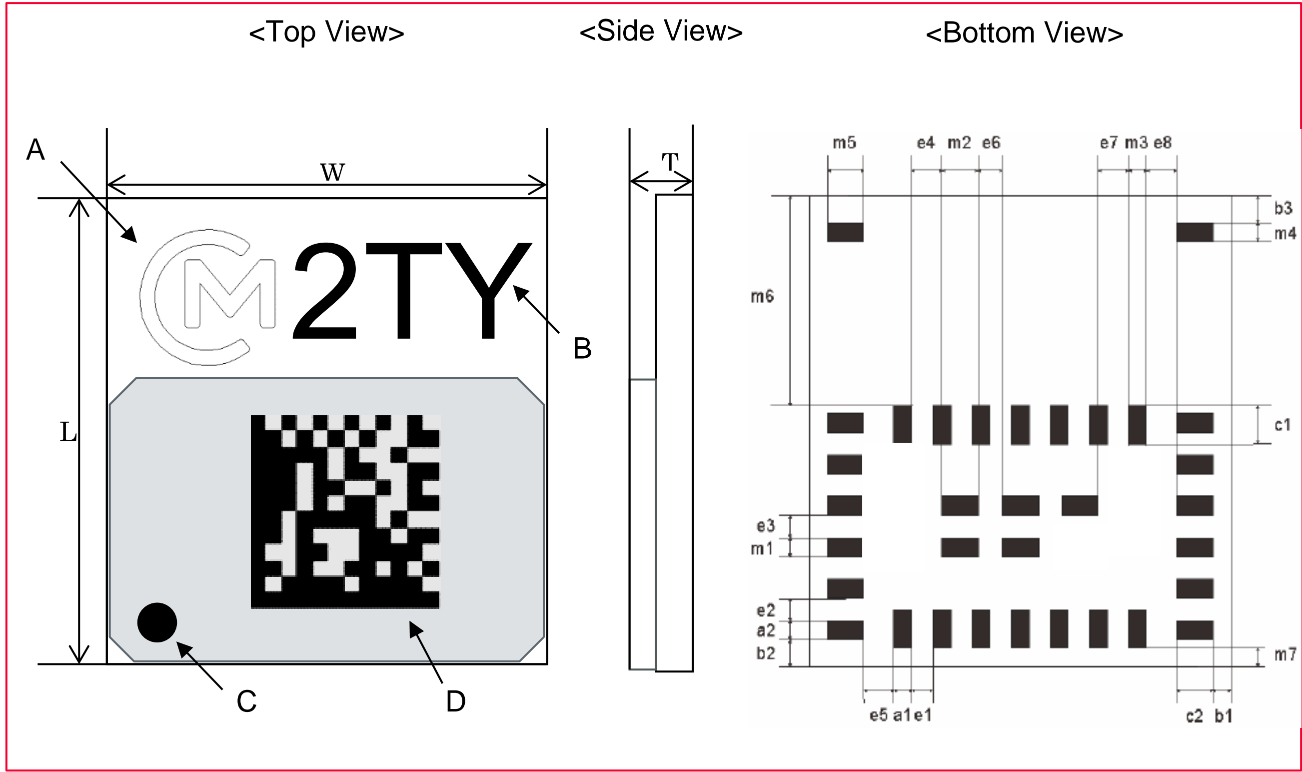


Table 3 describes the markings and meanings.

Table 3: Markings and Meanings

Mark	Dimensions
A	Murata Logo
B	Module Type
C	Pin 1 Marking
D	2D Code

Table 4 describes the markings and dimensions.

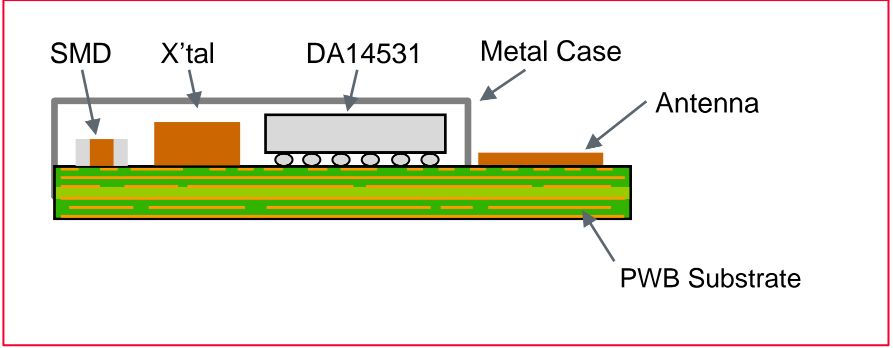
Table 4: Markings and Dimensions

Mark	Dimensions	Mark	Dimensions	Mark	Dimensions
L	7.4 +/- 0.25	W	7.0 +/- 0.25	T	1.3 maximum
a1	0.3 +/- 0.1	a2	0.3 +/- 0.1	b1	0.3 +/- 0.2
b2	0.425 +/- 0.2	b3	0.425 +/- 0.2	c1	0.6 +/- 0.1
c2	0.6 +/- 0.1	e1	0.35 +/- 0.1	e2	0.35 +/- 0.1
e3	0.35 +/- 0.1	e4	0.5 +/- 0.1	e5	0.5 +/- 0.1
e6	0.4 +/- 0.1	e7	0.5 +/- 0.1	e8	0.5 +/- 0.1
m1	0.3 +/- 0.1	m2	0.6 +/- 0.1	m3	0.3 +/- 0.1
m4	0.3 +/- 0.1	m5	0.6 +/- 0.1	m6	3.3 +/- 0.2
m7	0.3 +/- 0.2				

Structure

Figure 3 shows the module structure.

Figure 3: Structure



Pin Layout

Figure 4 shows the pin layout.

Figure 4: Pin Layout

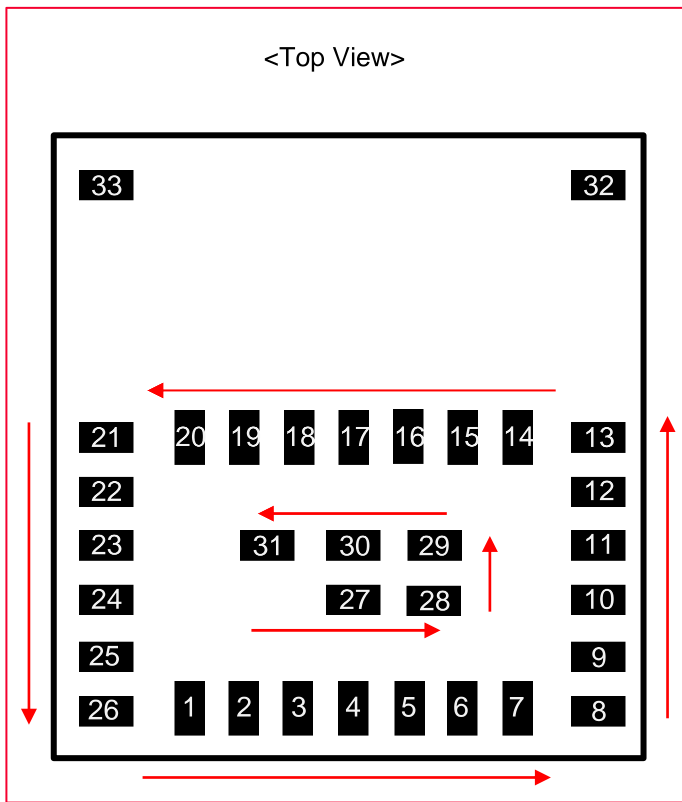


Table 5 lists the pin names.

Table 5: Pins

No.	Terminal Name	No.	Terminal Name	No.	Terminal Name	No.	Terminal Name
1	NC	10	P0_9	19	GND	28	GND
2	VBAT	11	P0_8	20	GND	29	GND
3	GND	12	GND	21	P0_6	30	GND
4	P0_1	13	NC	22	P0_5	31	GND
5	P0_2	14	NC	23	P0_11	32	NC
6	P0_3	15	GND	24	P0_10	33	NC

No.	Terminal Name	No.	Terminal Name	No.	Terminal Name	No.	Terminal Name
7	P0_4	16	GND	25	P0_0		
8	GND	17	GND	26	GND		
9	P0_7	18	GND	27	GND		

Table 6 describes the pins.

Table 6: Pin Descriptions

No.	Terminal Name	Connection to IC Pin Name	Type	Reset State	Description
1	NC				No Connection. (Internal use)
2	VBAT	VBAT_HIGH	Power		Power supply
3	GND	GND	GND		Ground
4	P0_1	P0_1	DIO (Type B)	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
		ADC0	AI		INPUT. Analog to Digital Converter input 0.
5	P0_2	P0_2	DIO (Type B)	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
		ADC1	AI		INPUT. Analog to Digital Converter input 1.
		SWCLK	DIO		INPUT JTAG clock signal (by default).
6	P0_3	P0_3	DIO (Type B)	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down. Check GP_DATA_REG[P03_P04_FILT_DIS] for correct pad filter settings.
		XTAL32kp	AI		INPUT. Analog input of the XTAL32K crystal oscillator
			DI		INPUT. Digital input for an external clock (square wave).
7	P0_4	P0_4	DIO (Type B)	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
		XTAL32km	AO		OUTPUT. Analog output of the XTAL32K crystal oscillator.
8	GND	GND			Ground
9	P0_7	P0_7	DIO (Type A)	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
		ADC3	AI		INPUT. Analog to Digital Converter input 3.
10	P0_9	P0_9	DIO (Type A)	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset.

No.	Terminal Name	Connection to IC Pin Name	Type	Reset State	Description
					General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
11	P0_8	P0_8	DIO (Type A)	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
12	GND	GND			Ground
13	NC				Connect to the GND on the customer board.
14	NC				Connect to the GND on the customer board.
15	GND	GND			Ground
16	GND	GND			
17	GND	GND			
18	GND	GND			
19	GND	GND			
20	GND	GND	-	-	
21	P0_6	P0_6	DIO (Type A)	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
		ADC2	AI		INPUT. Analog to Digital Converter input 2.
22	P0_5	P0_5	DIO (Type B)	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
23	P0_11	P0_11	DIO (Type A)	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
24	P0_10	P0_10	DIO (Type A)	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
		SWDIO	DIO		INPUT/OUTPUT. JTAG Data input/output. Bidirectional data and control communication (by default).
25	P0_0	P0_0	DIO (Type B)	I-PD	NPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
		RST	DIO (Type B)		RST active high hardware reset (default).
26	GND	GND			Ground
27	GND	GND			
28	GND	GND			
29	GND	GND			
30	GND	GND			

No.	Terminal Name	Connection to IC Pin Name	Type	Reset State	Description
31	GND	GND			
32	NC				No connection
33	NC				

For differences between Type A and Type B GPIO pads, please refer to Dialog semiconductor, DA14531 Datasheet - “Types of GPIO Pads”.

7 Ratings

Table 7 describes the ratings.

Table 7: Rating

Parameter	Minimum	Maximum	Unit
Storage Temperature	-40	+85	°C
VBAT Supply Voltage	-0.2	3.6	V
Input voltage for all other pins	-0.2	3.6	V

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability. No damage assuming only one parameter is set at limit at a time with all other parameters are set within operating condition.

8 Operating Conditions

Table 8 describes the operating conditions.

Table 8: Operating Conditions

Parameter			Minimum	Typical	Maximum	Unit
Operating Temperature Range[1]			-40		+85	°C
Supply Voltage		VBAT[2]	1.8	3.0	3.3	V
		VBAT for OTP programming[3]	2.25		3.3	V
		VBAT for OTP reading	1.8		3.3	V
Input voltage for all other pins			-0.2		VBAT + 0.2	V
RF Load Impedance				50		Ω
Peak current	VBAT				10	mA

1 Please keep derating / margin as much as possible at extreme temperature.
2 Type 2TY works only in Buck mode.
3 Required temperature for programming is between -20°C and 70°C

9 Power Up Sequence

Figure 5 shows the power up sequence.

Figure 5: Power Up Sequence

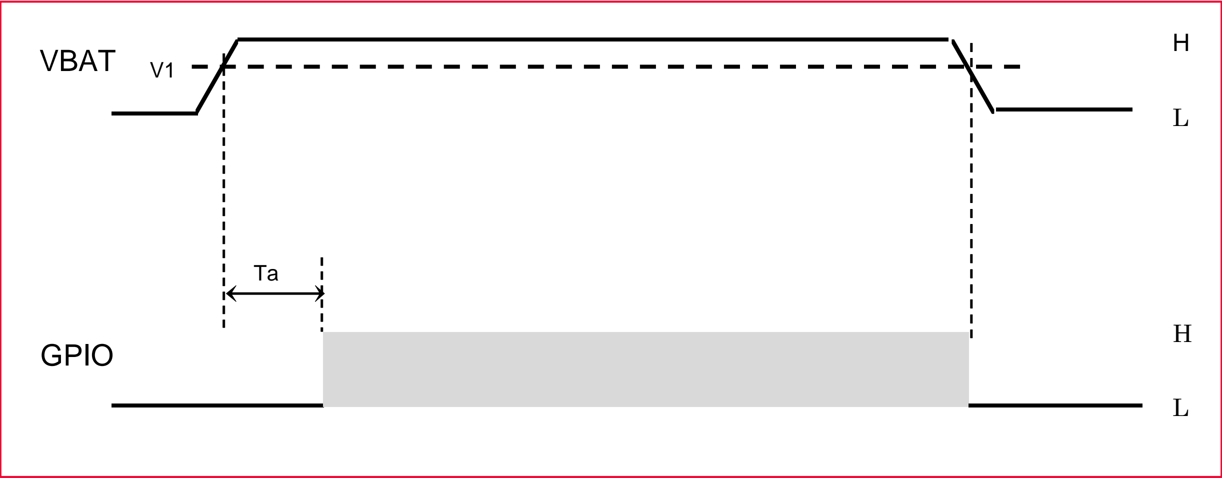


Figure 6 shows the reset and power cycle sequence.

Figure 6: Reset and Power Cycle Sequence

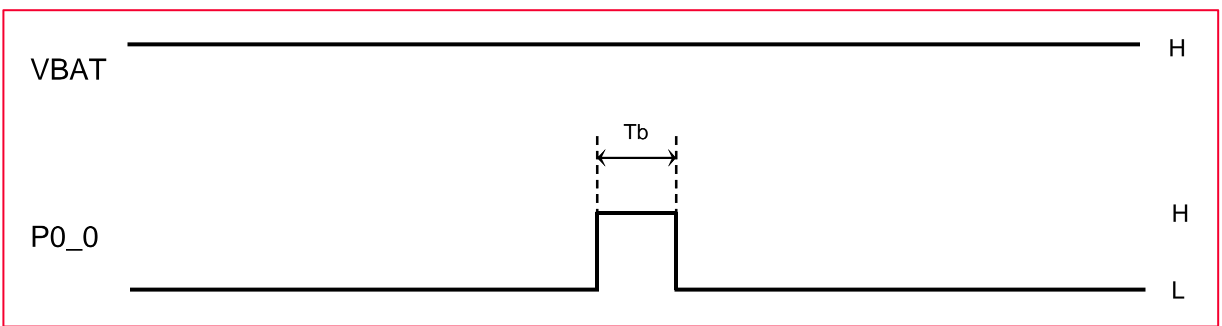


Table 9 describes the power sequence parameters.

Table 9: Power Sequence Parameters

Symbol	Description	Typical	Unit
Ta	Time between VBAT valid and GPIO enabled	Ta > 2.5	ms
Tb	Length of RST pulse	Tb > 15	µs
V1	Threshold voltage of VBAT	V1 ≥ 1.8	V

10 Digital I/O Requirements

Table 10 describes the digital I/O requirements.

Table 10: Digital I/O Requirements

Description	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Input low voltage	V_{DD} = 0.9 V (Active mode) V_{DD} = 0.75 V (Deep or Extended Sleep mode)[4]	V_{IL}			0.3 × VDD	V
Input high voltage		V_{IH}	0.7 × V_{DD}			V
Output low voltage	Active mode	V_{OL}			0.2 × VBAT	V
Output high voltage		V_{OH}	0.8 × VBAT			V
LOW level input current with internal pull up enabled	VI = VSS = 0V[5] VBAT = 3.0V	I_{IL_PU}	-180		60	µA
HIGH level input current with internal pull down enabled	VI = VBAT = 3.0V	I_{IH_PD}	60		180	µA

11 DC/RF Characteristics

Normal Conditions: +25 °C, VBAT = 3.0V

Table 11: 2 Mbps PHY Condition

Items	Contents			
Bluetooth specification (power class)	Version 5.1			
Channel frequency (spacing)	2402 to 2480 MHz (2MHz)			
Number of RF Channel	40			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx Mode		3.2		mA
• Rx Mode		2.4		mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Center Frequency	2402		2480	MHz
Channel Spacing		2		MHz
Number of RF channel		40		
Max Output power		2.5	4.9	dBm
Modulation Characteristics				
• $\Delta f1_{avg}$	225		275	kHz
• $\Delta f2_{max}$ (at 99.9%)	185			kHz
• $\Delta f2_{avg}$ / $\Delta f1_{avg}$	0.8			
Carrier frequency offset and drift				

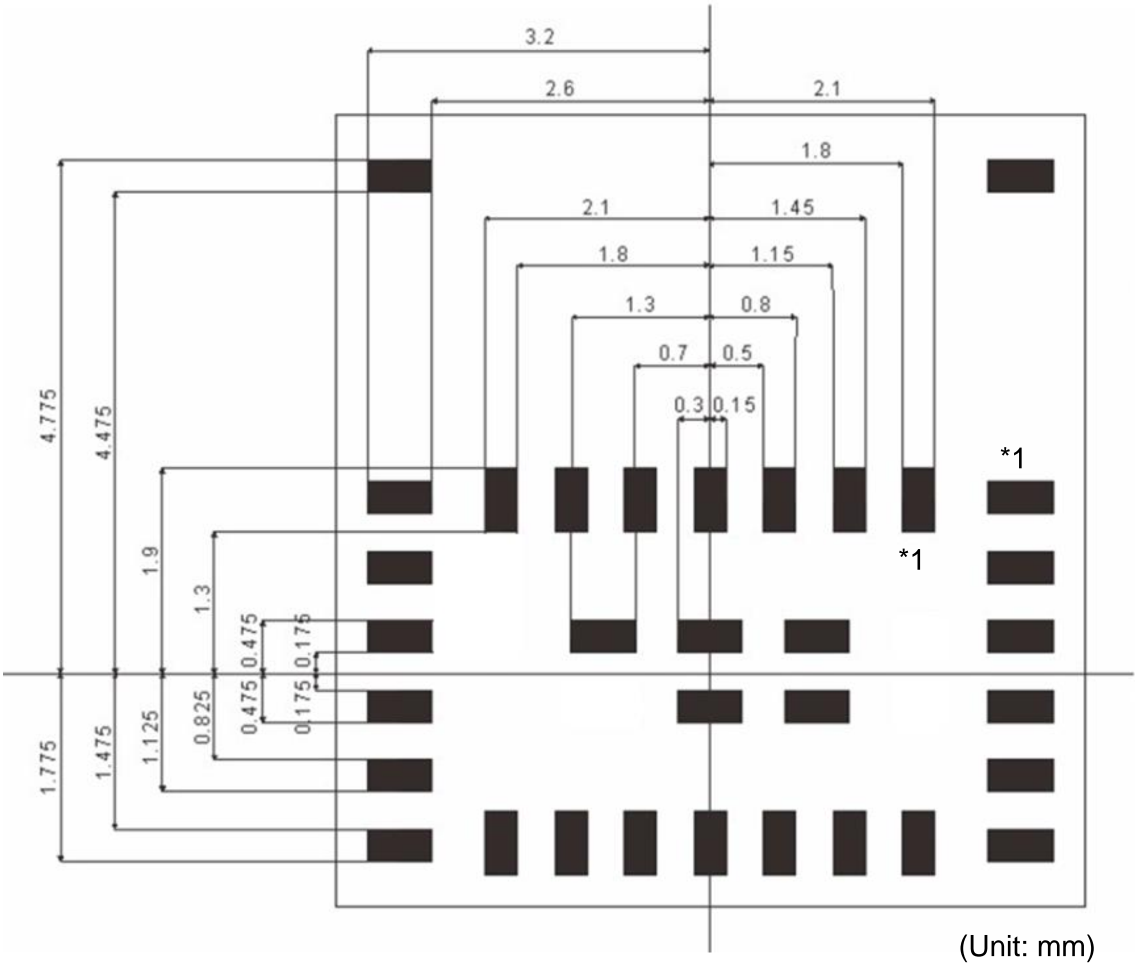
[4] VDD: IC internal power rail
[5] VSS: Digital ground

Items	Contents			
• Frequency offset			150	kHz
• Frequency drift			50	kHz
• Drift rate			20	kHz
Spurious Emissions				
• 30-47 MHz (BW = 100 kHz)			-36	dBm
• 47-74 MHz (BW = 100 kHz)			-54	dBm
• 74-87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5-118 MHz (BW = 100 kHz)			-54	dBm
• 118-174 MHz (BW = 100 kHz)			-36	dBm
• 174-230 MHz (BW = 100 kHz)			-54	dBm
• 230-470 MHz (BW = 100 kHz)			-36	dBm
• 470-862 MHz (BW = 100 kHz)			-54	dBm
• 862-1000 MHz (BW = 100 kHz)			-36	dBm
• 1000-12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Receiver sensitivity (PER < 30.8%)		-93	-70	dBm
Maximum input signal level (PER < 30.8%)	-10			dBm
PER Report Integrity (-30 dBm input)	-50		65.4	%

12 Land Patterns

Figure 7 shows the land patterns.

Figure 7: Land Patterns



*1 = Pin No.13 and No.14 are NC pins, but please connect to the GND on the customer board

13 Reference Circuit

This section describes reference circuit configurations using internal OTP and external flash.

13.1 Configuration Using Internal OTP

Figure 8 shows the reference circuit configuration using internal OTP.

Figure 8: Configuration Using Internal OTP

- Connection is necessary for software debugging in your product via J-Link.
    - OTP writing can also be done using J-Link.
    - RST input logic should be inverted externally if J-Link reset is enabled.
- 12 GPIOs (P0_0 to P0_11) are available for multipurpose use.
    - P0_1 to P0_3, P0_6 and P0_7 can be used for analog input.

13.2 Configuration Using External Flash

Figure 9 shows the reference circuit configuration using external flash.

Figure 9: Configuration Using External Flash

- Connection is necessary for software debugging in your product via J-Link.
  - OTP writing can also be done using J-Link.
  - RST input logic should be inverted externally if J-Link reset is enabled.

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14 Tape and Reel Packing

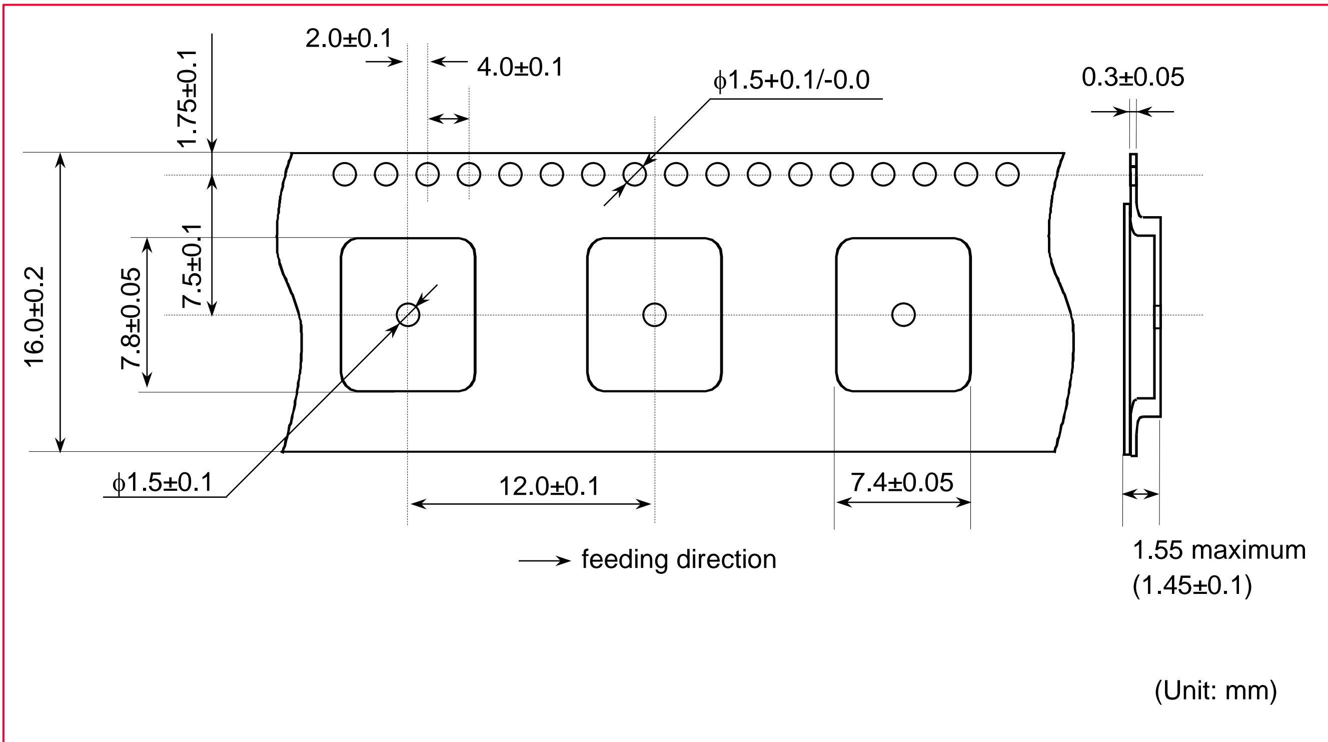
This section provides the general specifications for tape and reel packing.

14.1 Dimensions of Tape (Plastic Tape)

Figure 10 is a graphical representation of the tape dimension (plastic tape).

Cumulative tolerance of maximum 40.0 ± 0.15 mm every 10 pitches.

Figure 10: Dimension of Tape (Plastic Tape)



14.2 Dimension of Reel

Figure 11 shows the dimensions of reel in millimeters.

Figure 11: Dimensions of Reel

17.5

2±0.5

Φ13±2

(Φ100)

(Φ330)

22.5 max.

(Unit: mm)

14.3 Taping Diagrams

Figure 12 show the taping diagrams.

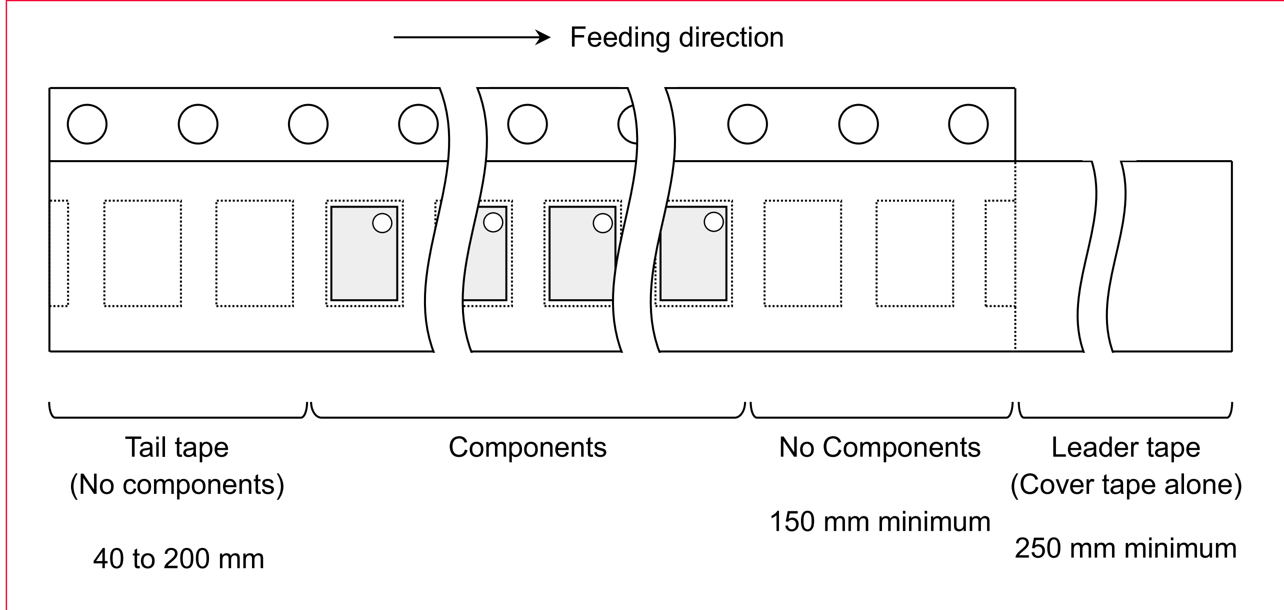
Figure 12: Taping Diagrams

Mark	Description
1	Feeding hole. As specified in Dimensions of Tape (Plastic tape).
2	Hole for Chip. As specified in Dimensions of Tape (Plastic tape).
3	Cover tape. 62 μm in thickness.
4	Base tape. As specified in Dimensions of Tape (Plastic tape).

14.4 Leader and Tail Tape

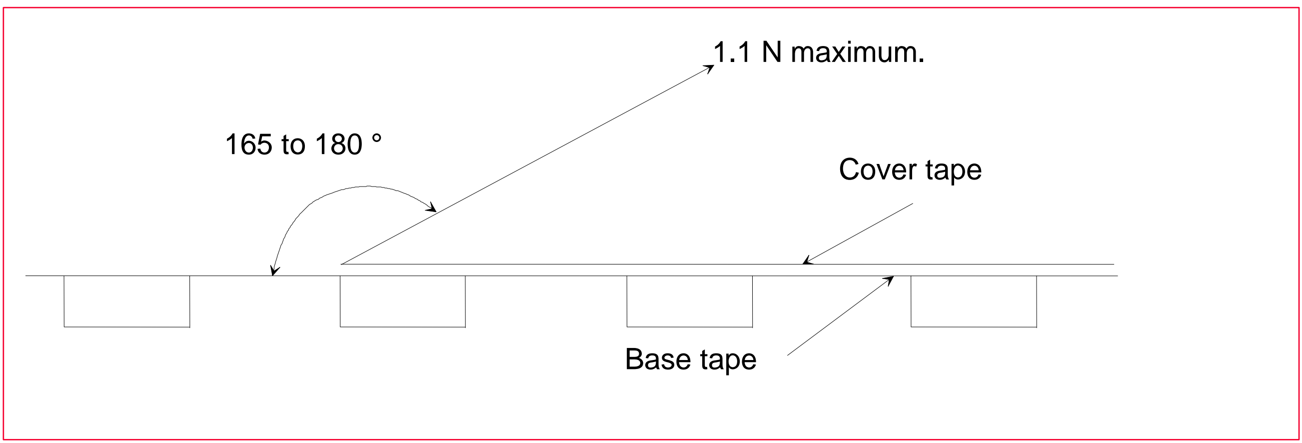
Figure 13 shows the leader and tail tape.

Figure 13: Leader and Tail Tape



- The tape for chips is wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.
- The cover tape and base tape are not adhered at no components area for 250 millimeters minimum.
- Tear off strength against pulling of cover tape : 5N minimum.
- Packaging unit : 1000pcs./ reel
- Material :
  - Base tape: Plastic
  - Real: Plastic
  - Cover tape, cavity tape and reel are made the anti-static processing.
- Peeling of force: 1.1N maximum in the direction of peeling as shown in **Figure 14**.

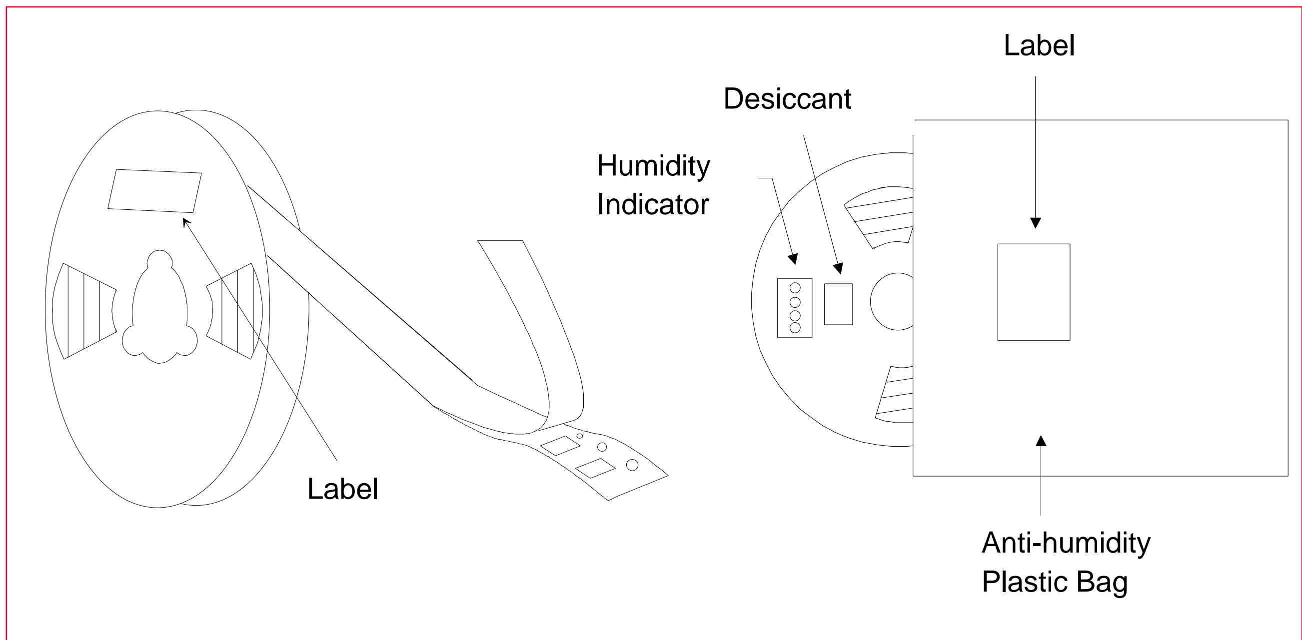
Figure 14: Peeling Force



14.5 Packaging (Humidity Proof Packing)

Figure 15 shows the humidity proof packaging.

Figure 15: Packaging



Tape and reel must be sealed with the anti-humidity plastic bag. The bag contains the desiccant and the humidity indicator.

14.6 Certification Label

Figure 16 shows the certification label.

Figure 16: Certification Label

This label is an example.

Please check the Section 5 for each certification number.

The above label is attached on the anti-humidity Plastic Bag.

15 Notice

15.1 Storage Conditions

- Please use this product within 6 months after receipt.
- The product shall be stored without opening the packing under the ambient temperature from 5 to 35 °C and humidity from 20 ~ 70 %RH (Packing materials, in particular, may be deformed at the temperature over 40 °C).
- The product left more than 6 months after reception; it needs to be confirmed the solderability before used.
- The product must be stored in noncorrosive gas (Cl_2, NH_3, SO_2, NO_X, etc.).
- Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object and dropping the product, must not be applied in order not to damage the packing materials.
- This product is applicable to MSL3 (Based on IPC/JEDEC J-STD-020)
- After the packing opened, the product must be stored at <30 °C / <60 %RH and the product must be used within 168 hours after opening.

- When the color of the indicator in the packing changed, the product shall be baked before soldering.
- Baking condition: 125 +5/-0 °C, 24 hours, 1 time
- The products must be baked on the heat-resistant tray because the material (Base Tape, Reel Tape and Cover Tape) is not heat-resistant.

15.2 Handling Conditions

- Be careful in handling or transporting products because excessive stress or mechanical shock may break products.
- Handle with care if products may have cracks or damages on their terminals. If there is any such damage, the characteristics of products may change. Do not touch products with bare hands that may result in poor solder ability and destroy by static electrical charge.

15.3 Standard PCB Design (Land Pattern and Dimensions)

- All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.
- The recommended land pattern and dimensions is as Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set. When using non-standard lands, contact Murata beforehand.

15.4 Notice for Chip Placer

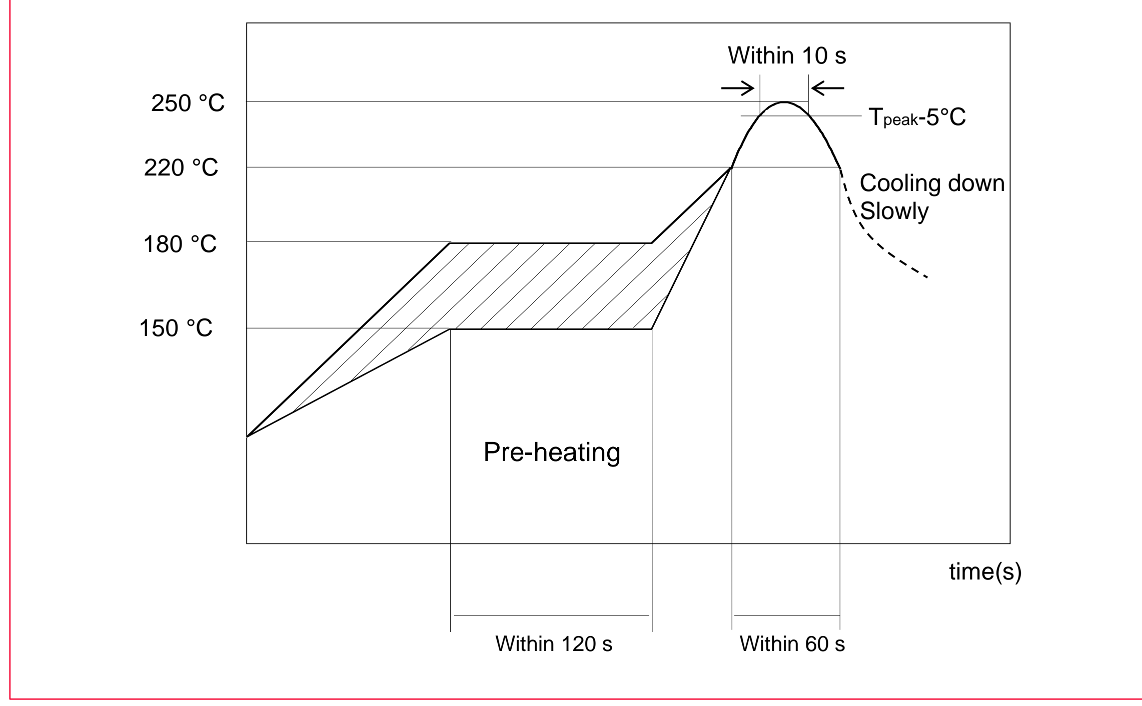
When placing products on the PCB, products may be stressed and broken by uneven forces from a worn-out chucking locating claw or a suction nozzle. To prevent products from damages, be sure to follow the specifications for the maintenance of the chip placer being used. For the positioning of products on the PCB, be aware that mechanical chucking may damage products.

15.5 Soldering Conditions

The recommendation conditions of soldering are as in the following figure.

Soldering must be carried out by the above-mentioned conditions to prevent products from damage. Set up the highest temperature of reflow within 260 °C. Contact Murata before use if concerning other soldering conditions.

Figure 17: Reflow Soldering Standard Conditions (Example)



Please use the reflow within 2 times.

Use rosin type flux or weakly active flux with a chlorine content of 0.2 wt % or less.

15.6 Cleaning

Since this Product is Moisture Sensitive, any cleaning is not recommended. If any cleaning process is done the customer is responsible for any issues or failures caused by the cleaning process.

15.7 Operational Environment Conditions

Products are designed to work for electronic products under normal environmental conditions (ambient temperature, humidity, and pressure). Therefore, products have no problems to be used under similar conditions to the above-mentioned. However, if products are used under the following circumstances, it may damage products and leakage of electricity and abnormal temperature may occur.

- In an atmosphere containing corrosive gas (Cl_2, NH_3, SO_X, NO_X etc.).
- In an atmosphere containing combustible and volatile gases.
- Dusty place.
- Direct sunlight place.
- Water splashing place.
- Humid place where water condenses.
- Freezing place.

If there are possibilities for products to be used under the preceding clause, consult with Murata before actual use.

Do not apply static electricity or excessive voltage while assembling and measuring, as it might be a cause of degradation or destruction to apply static electricity to products.

16 Preconditions to Use Our Products

PLEASE READ THIS NOTICE BEFORE USING OUR PRODUCTS.

Please make sure that your product has been evaluated and confirmed from the aspect of the fitness for the specifications of our product when our product is mounted to your product.

All the items and parameters in this product specification/datasheet/catalog have been prescribed on the premise that our product is used for the purpose, under the condition and in the environment specified in this specification. You are requested not to use our product deviating from the condition and the environment specified in this specification.

Please note that the only warranty that we provide regarding the products is its conformance to the specifications provided herein. Accordingly, we shall not be responsible for any defects in products or equipment incorporating such products, which are caused under the conditions other than those specified in this specification.

WE HEREBY DISCLAIM ALL OTHER WARRANTIES REGARDING THE PRODUCTS, EXPRESS OR IMPLIED, INCLUDING WITHOUT LIMITATION ANY WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE, THAT THEY ARE DEFECT-FREE, OR AGAINST INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS.

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The product shall not be used in any application listed below which requires especially high reliability for the prevention of such defect as may directly cause damage to the third party's life, body or property. You acknowledge and agree that, if you use our products in such applications, we will not be responsible for any failure to meet such requirements. Furthermore, YOU AGREE TO INDEMNIFY AND DEFEND US AND OUR AFFILIATES AGAINST ALL CLAIMS, DAMAGES, COSTS, AND EXPENSES THAT MAY BE INCURRED, INCLUDING WITHOUT LIMITATION, ATTORNEY FEES AND COSTS, DUE TO THE USE OF OUR PRODUCTS AND THE SOFTWARE IN SUCH APPLICATIONS.

- Aircraft equipment.
- Aerospace equipment.

- Undersea equipment.
- Power plant control equipment.
- Medical equipment.
- Traffic signal equipment.
- Burning / explosion control equipment.
- Disaster prevention / crime prevention equipment.
- Transportation equipment (vehicles, trains, ships, elevator, etc.).
- Application of similar complexity and/ or reliability requirements to the applications listed in the above.

We expressly prohibit you from analyzing, breaking, reverse-engineering, remodeling altering, and reproducing our product. Our product cannot be used for the product which is prohibited from being manufactured, used, and sold by the regulations and laws in the world.

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Please do not use our products, our technical information and other data provided by us for the purpose of developing of mass-destruction weapons and the purpose of military use.

Moreover, you must comply with "foreign exchange and foreign trade law", the "U.S. export administration regulations", etc.

Please note that we may discontinue the manufacture of our products, due to reasons such as end of supply of materials and/or components from our suppliers.

By signing on specification sheet or approval sheet, you acknowledge that you are the legal representative for your company and that you understand and accept the validity of the contents herein. When you are not able to return the signed version of specification sheet or approval sheet within 30 days from receiving date of specification sheet or approval sheet, it shall be deemed to be your consent on the content of specification sheet or approval sheet. Customer acknowledges that engineering samples may deviate from specifications and may contain defects due to their development status. We reject any liability or product warranty for engineering samples. In particular we disclaim liability for damages caused by

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- Deviation or lapse in function of engineering sample,
- Improper use of engineering samples.

We disclaim any liability for consequential and incidental damages.

If you can’t agree with the above contents, please contact sales.

Revision History

Revision	Date	Description	Change Description
	Aug 30, 2021		Initial Release
A	Dec 02, 2021	• 6. Dimensions, Marking and Terminal Configurations Pin Layout • 12.Land Patterns	• Corrected the description of Pin No13 and 14 • Added comment

B	Jan 12, 2022	• DC/RF Characteristics
		• 13. Reference Circuit
		  • 13.1 Configuration using internal OTP
		  • 13.2 Configuration using external flash
			• Revised the table
			• Added the reference circuit
			• Added the reference circuit

C	May 20, 2020	• 13. Reference Circuit
		  • 13.1 Configuration using internal OTP
		  • 13.2 Configuration using external flash
			• Added comment
			• Added comment

D	Mar 02, 2023	• 5. Certification Information
		  • 5.1 Radio Certification
		  • 5.2 Bluetooth Qualification
			• Added the certification No.
			• Added QDID

E	Sep 28, 2023	• 11. DC/RF Characteristics	Added Output power Max
F	Nov 28, 2023	• All sections	Updated to new document template

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