

# Application Note

## ***Suitable circuit conditions for muRata's crystal on PN544/PN65N***

Issued by

**muRata**

Checked by

Confidential

# Application Note

## Purpose of this application note

For the customer who is trying to embed NFC function by PN544/PN65N\* (released by NXP), muRata will provide information of

1. Suitable crystal part number by muRata
2. Optimized circuit conditions for oscillation circuit

to save customer's time and resources for evaluation above.

\* Both of PN544 and PN65N are IC for NFC, and oscillation characteristics on both ICs are same.

## Index

1. Spec. of crystal by muRata
2. Optimized circuit conditions
3. Oscillation characteristics
4. Circuit conditions without  $R_d$

# Application Note

## 1. Crystal part number for PN544

### **XRCGB27M120F3M10R0**

Small size (2.0x1.6x0.7mm) crystal for NFC.  
Refer table below for specification.

### Spec. of muRata's crystal

Parameter	Requirements by PN544/PN65N(*1)			Spec. of muRata's crystal			Judge
	Min	Typ	Max	Min	Typ	Max	
$f_{XTAL}$ [MHz] (*2)	27.107	27.12	27.133	27.118	27.12	27.122	✓
ESR [ohm] (*3)		50	100			80	✓
$C_{LOAD}$ [pF] (*4)		10			10		✓
$P_{XTAL}$ [uW] (*5)			100			300	✓

(\*1): Refer datasheet of PN544/PN65N

(\*2): Frequency tolerance by crystal.

Spec. of muRata's crystal above includes initial variation @25[deg.C] and drift by operating temperature range from -30 to 85[deg.C].

(\*3): Equivalent Series Resistance. Resistance of the crystal.

(\*4): Specified capacitance for frequency sorting on crystal.

(\*5): Withstand-ability for how high power the crystal can use by.

Refer oscillation characteristics data for actual power consumption on crystal.

***muRata's crystal meets all of requirements by PN544/PN65N!***

# Application Note

## 2. Optimized circuit conditions

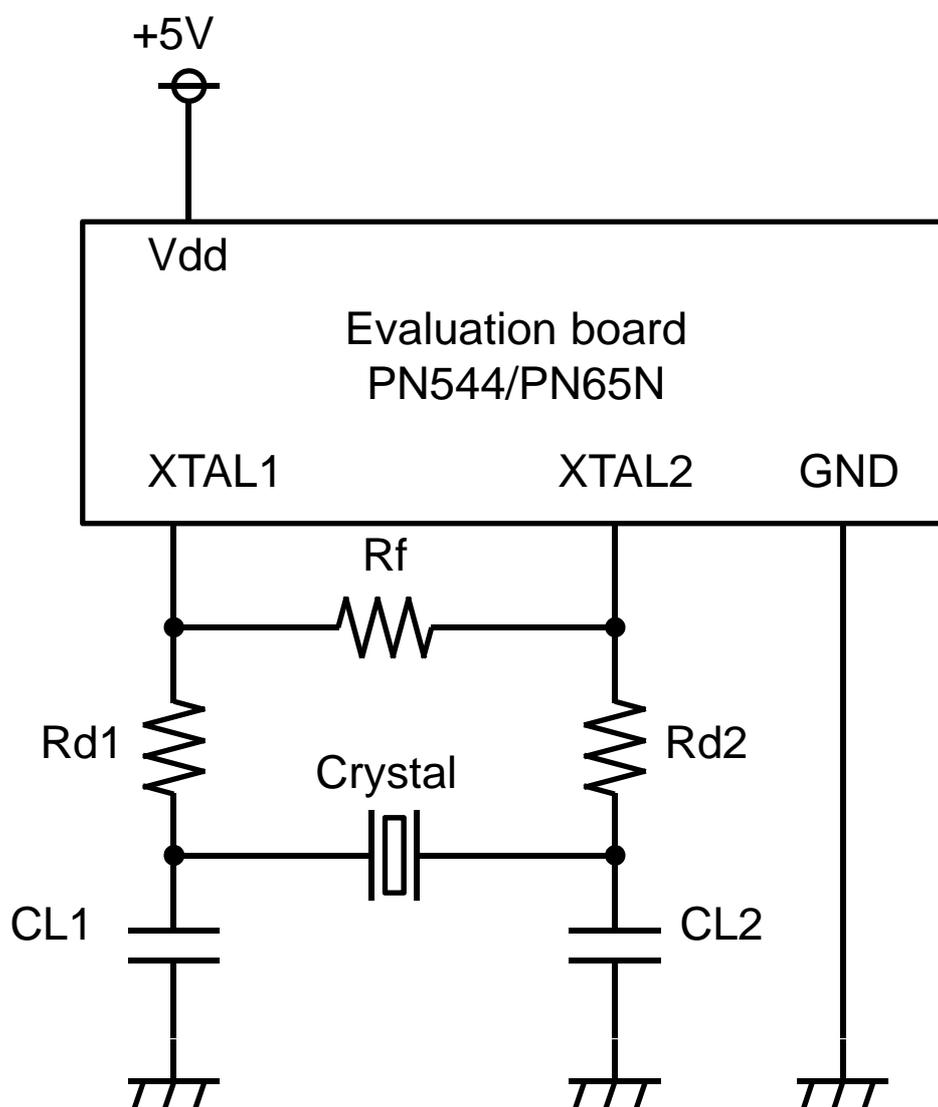


Figure of oscillation circuit

Symbol	Parameter	Optimized value
$R_f$	Feedback resistor	No mount
$R_{d1}$	Damping resistor at Xin	680 [ohm]
$R_{d2}$	Damping resistor at Xout	0 [ohm]
$CL1$	External capacitance	12 [pF]
$CL2$	External capacitance	12 [pF]

# Application Note

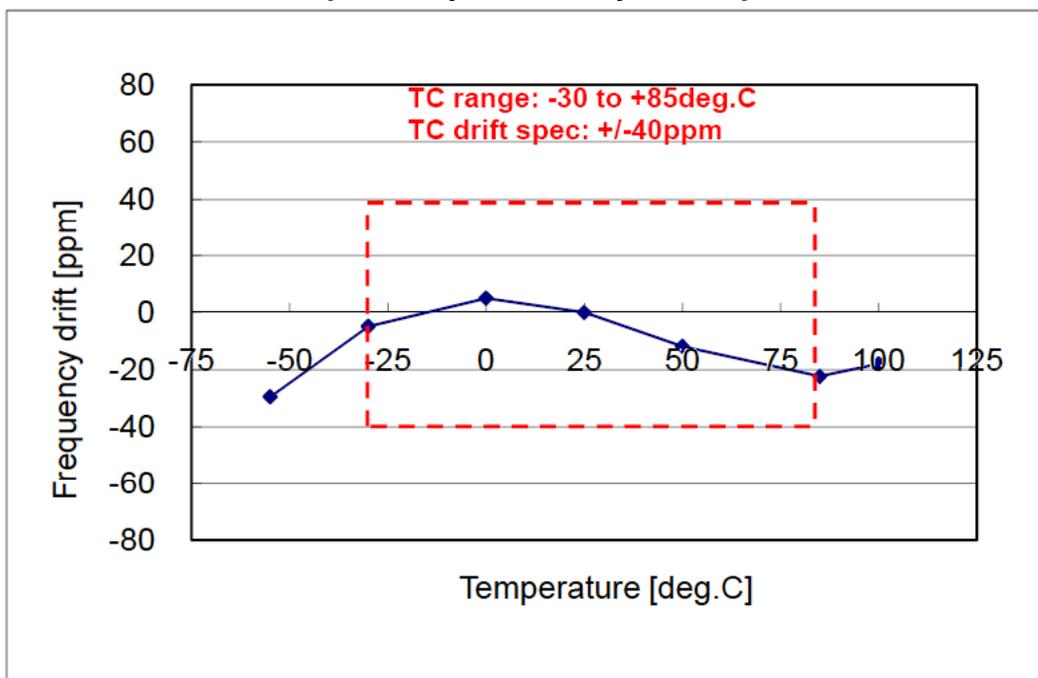
## 3. Oscillation characteristics

### Measured oscillation characteristics

Parameter	Measured results
Oscillation margin	5.5 [times]
Drive level	54 [ $\mu$ W]
Actual load capacitance	8.2 [pF]
Nominal frequency shift (from 27.12MHz)	+12ppm
Frequency drift by temperature	See below chart
Start up time of crystal	0.52 [ms]*

\* Refer to next page in detail

### Measured frequency drift by temperature



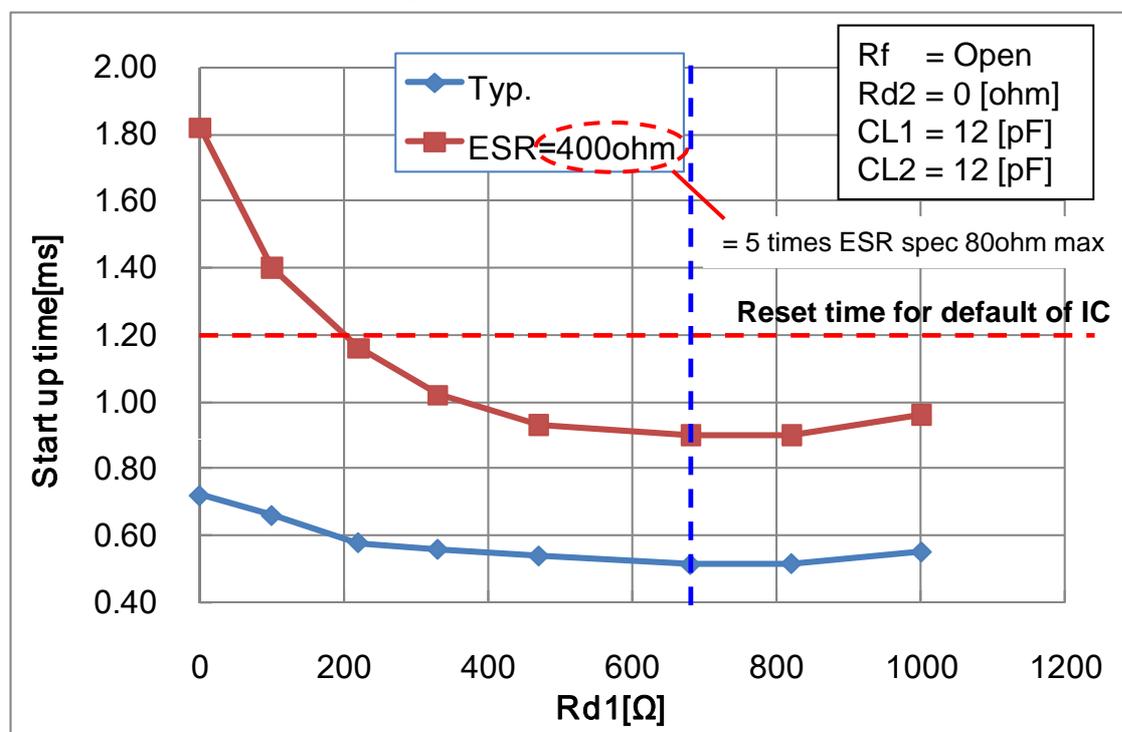
All of above results have been measured on evaluation board of PN65N from NXP, with optimized circuit conditions for XRCGB27M120F3M10R0.

Refer TCD-11-0235, issued by muRata, for more detail.

# Application Note

## <Start up time of crystal>

### Measured start up time of the crystal by Rd1



Adding resistor (Rd1) at input side (XTAL1) will help to shorten start up time of the oscillation.

Murata recommendable resistance value of Rd1 is 680 [ohm].

The IC default setting of reset time is approximately 1.2ms.

Murata confirmed the oscillation starts up within 1.2ms (much less than 1.2ms), also taking into account of necessary oscillation margin, under Murata's recommendable circuit conditions.

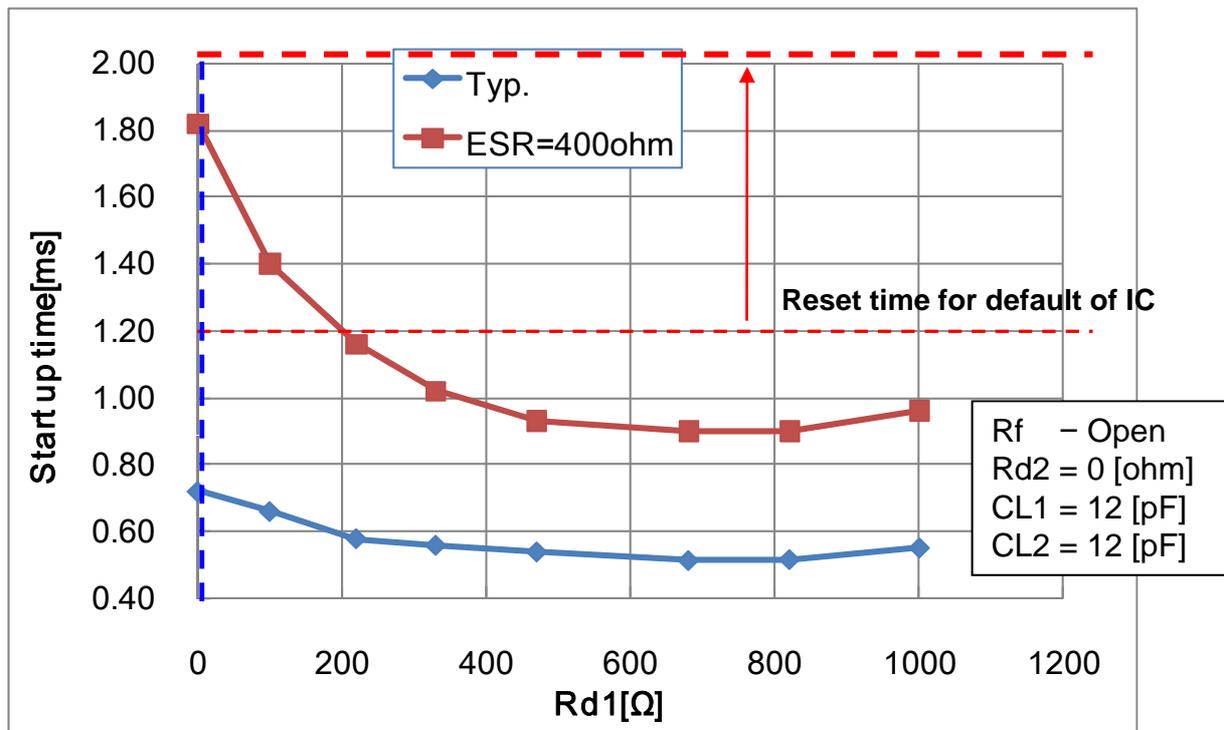
Murata judges that the oscillation is stable enough when the oscillation margin of over 5 times is secured in the negative resistance analysis. Please refer to the measurement result above. Start up time of our crystal at Rd1=680ohm is less than 1.2ms even if ESR of crystal with 400ohm, which is 5 times of ESR spec 80ohm max., is considered.

\* This results have been measured on evaluation board of PN65N by NXP with XRCGB27M120F3M10R0.

# Application Note

## 4. Circuit condition without Rd1

### Measured start up time of the crystal by Rd1



It is possible to omit Rd1 (Rd1=0 ohm) but changing the reset time setting may be required.

The default setting of reset time is 1.2ms.

Murata generally recommends to change the reset time setting to 2ms or longer in the case of omitting Rd1.

For consideration of changing the reset time setting, to check the oscillation start up time on the actual PCB would be more recommended because start up time may be different PCB by PCB.

The oscillation characteristics are shown in page 9.

This results have been measured on evaluation board of PN65N by NXP with XRCGB27M120F3M10R0.

# Application Note

## Circuit conditions at $R_{d1}=0\text{ohm}$

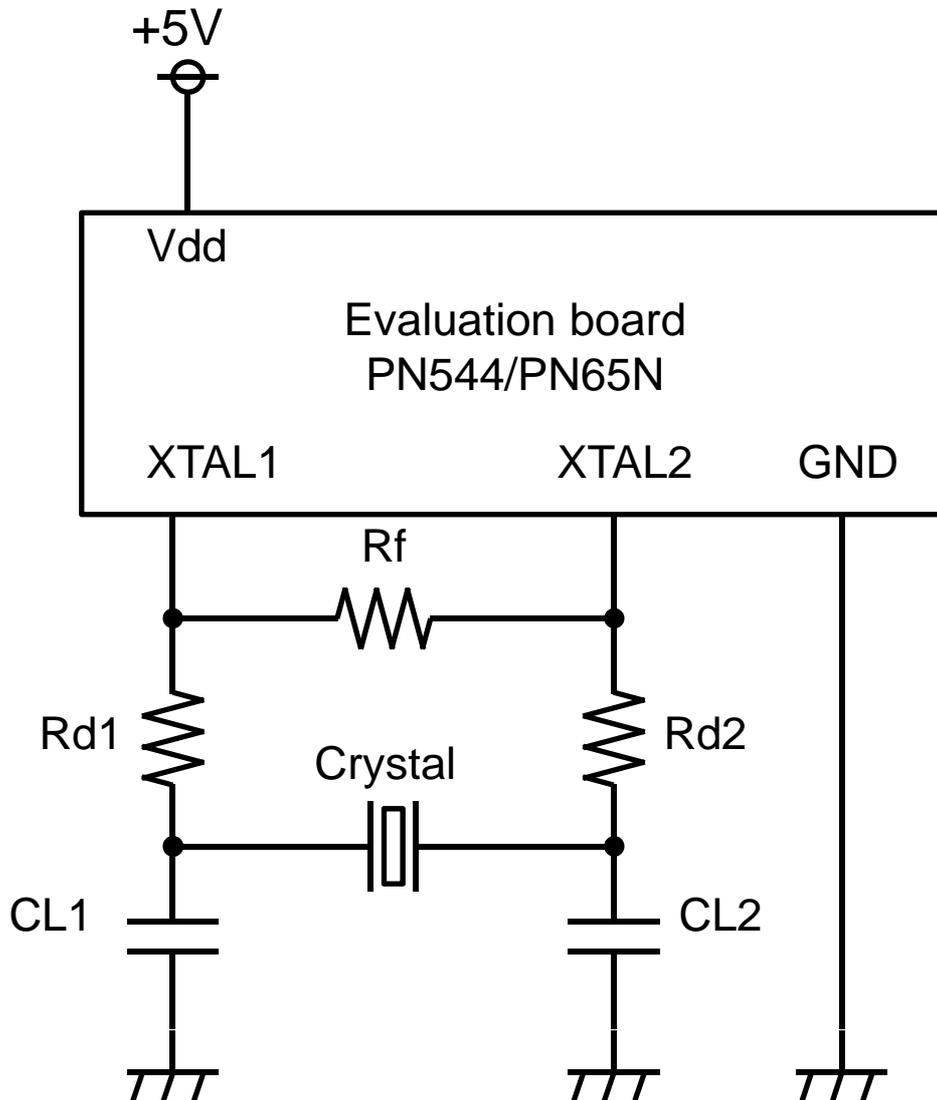


Figure of oscillation circuit

Symbol	Parameter	Circuit conditions
Rf	Feedback resistor	No mount
Rd1	Damping resistor at Xin	0 [ohm]
Rd2	Damping resistor at Xout	0 [ohm]
CL1	External capacitance	12 [pF]
CL2	External capacitance	12 [pF]

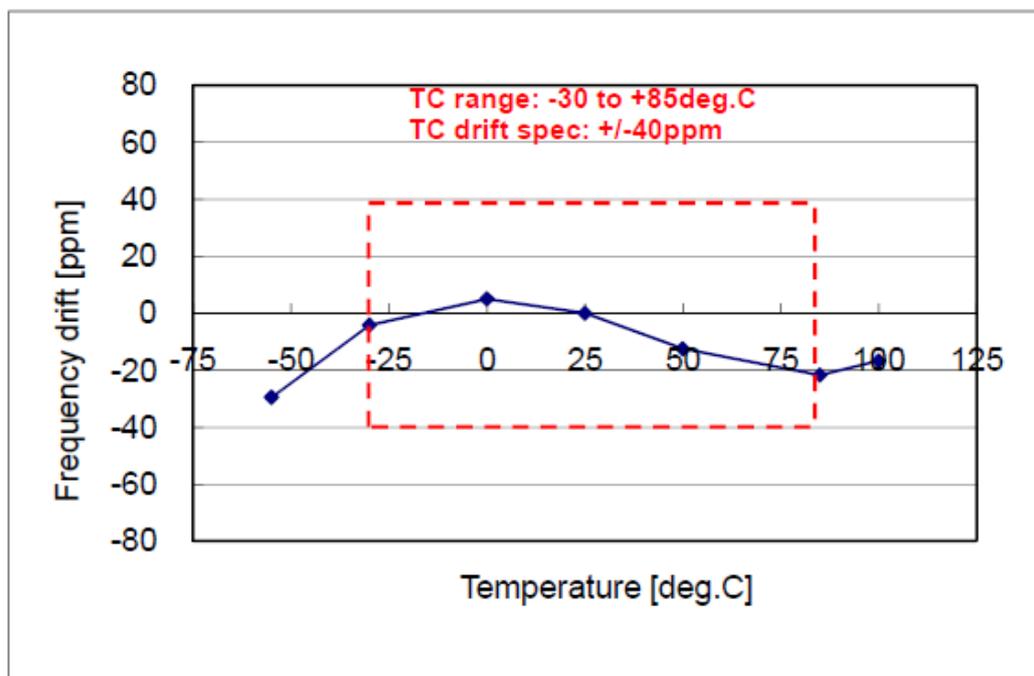
# Application Note

## Oscillation characteristics (Rd1=0ohm)

### Measured oscillation characteristics (Rd1=0ohm)

Parameter	Measured results
Oscillation margin	6.0 [times]
Drive level	52 [ $\mu$ W]
Actual load capacitance	8.1 [pF]
Nominal frequency shift (from 27.12MHz)	+17ppm
Frequency drift by temperature	See below chart
Start up time of crystal	0.72 [ms]

### Measured frequency drift by temperature (Rd1=0ohm)



All of above results have been measured on evaluation board of PN65N by NXP, with circuit conditions at Rd1=0ohm for XRCGB27M120F3M10R0.

Refer to TCD-11-0234, issued by muRata, for more detail.